

## CLAIMS

What is claimed is:

1        1.    An integrated circuit to interface to memory, the  
2 integrated circuit comprising:  
3            a first off chip driver calibration terminal to  
4 couple to an external pull-up resistor;  
5            a second off chip driver calibration terminal to  
6 couple to an external pull-down resistor;  
7            a first switch coupled between the first off chip  
8 driver calibration terminal and a voltage reference node;  
9 and  
10           a second switch coupled between the second off chip  
11 driver calibration terminal and the voltage reference  
12 node.

1        2.    The integrated circuit of claim 1, wherein  
2            the first switch and the second switch are  
3 selectively closed to generate an internal voltage  
4 reference on the voltage reference node with which an  
5 input signal may be compared in order to receive data.

1        3.    The integrated circuit of claim 2, wherein  
2            the first switch is selectively closed and the  
3 second switch is selectively opened to generate a pull-up

4 calibration voltage on the voltage reference node to  
5 calibrate an off-chip driver.

1 4. The integrated circuit of claim 3, wherein  
2 the first switch is selectively opened and the  
3 second switch is selectively closed to generate a pull-  
4 down calibration voltage on the voltage reference node to  
5 further calibrate the off-chip driver.

1 5. The integrated circuit of claim 1, further  
2 comprising:  
3 a plurality of input receivers each having a first  
4 input coupled to the voltage reference node and a second  
5 input coupled to a respective data terminal of a  
6 plurality of data terminals.

1 6. The integrated circuit of claim 5, wherein  
2 each input receiver includes  
3 a comparator having a first input coupled to the  
4 voltage reference node and a second input coupled to the  
5 respective data terminal, the data terminal to couple to  
6 an off-chip output driver for calibration.

1 7. The integrated circuit of claim 1, further  
2 comprising:  
3 a switch controller having a mode input, a first  
4 control output coupled to a control input of the first

5 switch, and a second control output coupled to a control  
6 input of the second switch, the switch controller to  
7 control the opening and closing of the first switch and  
8 the second switch in response to the mode input.

1 8. The integrated circuit of claim 7, wherein  
2 the first switch and the second switch are  
3 selectively closed to generate an internal voltage  
4 reference on the voltage reference node with which an  
5 input signal may be compared in order to receive data;  
6 the first switch is selectively closed and the  
7 second switch is selectively opened to generate a pull-up  
8 calibration voltage on the voltage reference node to  
9 calibrate an off-chip driver; and  
10 the first switch is selectively opened and the  
11 second switch is selectively closed to generate a pull-  
12 down calibration voltage on the voltage reference node to  
13 further calibrate the off-chip driver.

1 9. The integrated circuit of claim 1, wherein  
2 the integrated circuit is a memory controller.

1 10. The integrated circuit of claim 1, wherein  
2 the integrated circuit is a processor.

1 11. A method in an integrated circuit for interfacing to  
2 a memory, the method comprising:

3           if in an off-chip driver calibration mode for a  
4 pull-up, then  
5           selecting a pull-up calibration terminal to be  
6 coupled to a voltage reference node to provide a  
7 pull-up calibration voltage thereon, and  
8           calibrating a pull-up of an off chip driver;  
9           if in an off-chip driver calibration mode for a  
10 pull-down, then  
11          selecting a pull-down calibration terminal to  
12 be coupled to the voltage reference node to provide  
13 a pull-down calibration voltage thereon, and  
14          calibrating a pull-down of the off chip driver;  
15 and,  
16 if in a normal mode to receive data, then  
17          selecting the pull-up calibration terminal and  
18 the pull-down calibration terminal to be coupled to  
19 the voltage reference node to provide a reference  
20 voltage thereon, and  
21          receiving data from a data terminal.

1       12. The method of claim 11 further comprising:  
2 prior to selecting, calibrating and receiving,  
3       coupling an external pull-up resistor to the  
4 pull-up calibration terminal; and  
5       coupling an external pull-down resistor to the  
6 pull-down calibration terminal.

1        13. The method of claim 11, wherein  
2                the receiving data from the data terminal includes  
3                comparing the reference voltage on the voltage  
4 reference node with an incoming signal on the data  
5 terminal.

1        14. The method of claim 13, wherein  
2                the calibrating of the pull-up of the off chip  
3 driver includes  
4                comparing the pull-up calibration voltage on the  
5 voltage reference node with an incoming signal on the  
6 data terminal.

1        15. The method of claim 14, wherein  
2                the calibrating of the pull-down of the off chip  
3 driver includes  
4                comparing the pull-down calibration voltage on the  
5 voltage reference node with an incoming signal on the  
6 data terminal.

1        16. A system comprising:  
2                a processor for executing instructions and  
3 processing data;  
4                a double data rate memory device to store data from  
5 the processor and to read data to the processor;

6           an external pull-up resistor having a first end  
7       coupled to a first power supply terminal;  
8           an external pull-down resistor having a first end  
9       coupled to a second power supply terminal; and  
10          a memory controller coupled between the double data  
11       rate memory device and the processor, the memory  
12       controller including  
13           a pull-up calibration terminal coupled to a  
14          second end of the external pull-up resistor,  
15           a pull-down calibration terminal coupled to a  
16          second end of the external pull-down resistor,  
17           a voltage reference node,  
18           a first switch having a first switch connection  
19          coupled to the pull-up calibration terminal and a  
20          second switch connection coupled to the voltage  
21          reference node, and  
22           a second switch having a first switch  
23          connection coupled to the pull-down calibration  
24          terminal and a second switch connection coupled to  
25          the voltage reference node.

1       17. The system of claim 16, wherein  
2           the memory controller is an integrated circuit  
3       separate from the processor.

1       18. The system of claim 16, wherein

2           the processor is an integrated circuit and includes  
3           the memory controller.

1           19. The system of claim 16, wherein  
2           the memory controller further includes  
3           a switch controller having a mode input, a  
4           first control output coupled to a control input of  
5           the first switch, and a second control output  
6           coupled to a control input of the second switch, the  
7           switch controller to control the opening and closing  
8           of the first switch and the second switch in  
9           response to the mode input.

1           20. The system of claim 19, wherein  
2           the first switch and the second switch are  
3           selectively closed to generate an internal voltage  
4           reference on the voltage reference node with which an  
5           input signal may be compared in order to receive data;  
6           the first switch is selectively closed and the  
7           second switch is selectively opened to generate a pull-up  
8           calibration voltage on the voltage reference node to  
9           calibrate a driver of the DDR memory device; and  
10          the first switch is selectively opened and the  
11          second switch is selectively closed to generate a pull-  
12          down calibration voltage on the voltage reference node to  
13          further calibrate the driver of the DDR memory device.

1        21. A processor for a computer system, the processor  
2 including:  
3            a memory controller to interface to memory, the  
4 memory controller having  
5            a pull-up calibration terminal to couple to an  
6 external pull-up resistor,  
7            a pull-down calibration terminal to couple to  
8 an external pull-down resistor,  
9            a voltage reference node,  
10           a first switch coupled between the pull-up  
11 calibration terminal and the voltage reference node,  
12 and  
13           a second switch coupled between the pull-down  
14 calibration terminal and the voltage reference node.

1        22. The processor of claim 21, wherein  
2           the memory controller further has  
3           a switch controller having a mode input, a  
4 first control output coupled to a control input of  
5 the first switch, and a second control output  
6 coupled to a control input of the second switch, the  
7 switch controller to control the opening and closing  
8 of the first switch and the second switch in  
9 response to the mode input.

1        23. The processor of claim 22, wherein



2           the first switch and the second switch are  
3           selectively closed to generate an internal voltage  
4           reference on the voltage reference node with which an  
5           input signal may be compared in order to receive data  
6           from a driver of a DDR memory device;  
7           the first switch is selectively closed and the  
8           second switch is selectively opened to generate a pull-up  
9           calibration voltage on the voltage reference node to  
10          calibrate the driver of the DDR memory device; and  
11          the first switch is selectively opened and the  
12          second switch is selectively closed to generate a pull-  
13          down calibration voltage on the voltage reference node to  
14          further calibrate the driver of the DDR memory device.

1          24. A packaged integrated circuit to interface to  
2 memory, the packaged integrated circuit comprising:  
3           a first off-chip driver calibration terminal to  
4           couple to a first external resistor;  
5           a second off-chip driver calibration terminal to  
6           couple to a second external resistor;  
7           a first plurality of field effect transistors having  
8           sources coupled in parallel together to the first off-  
9           chip driver calibration terminal and drains coupled in  
10          parallel together to a voltage reference node; and  
11          a second plurality of field effect transistors  
12          having drains coupled in parallel together to the second

13 off-chip driver calibration terminal and sources coupled  
14 in parallel together to the voltage reference node.

1 25. The packaged integrated circuit of claim 24 wherein  
2 the first plurality of field effect transistors and  
3 the second plurality of field effect transistors are p-  
4 channel field effect transistors.

1 26. The packaged integrated circuit of claim 24 wherein  
2 the first plurality of field effect transistors and  
3 the second plurality of field effect transistors are n-  
4 channel field effect transistors.

1 27. The packaged integrated circuit of claim 24 wherein  
2 the first plurality of field effect transistors are  
3 p-channel field effect transistors, and  
4 the second plurality of field effect transistors are  
5 n-channel field effect transistors.

1 28. The packaged integrated circuit of claim 24 wherein  
2 the first plurality of field effect transistors are  
3 n-channel field effect transistors, and  
4 the second plurality of field effect transistors are  
5 p-channel field effect transistors.

1 29. The packaged integrated circuit of claim 24 wherein

2           the first plurality of field effect transistors are  
3           p-channel field effect transistors and n-channel field  
4           effect transistors having sources coupled in parallel  
5           together and drains coupled in parallel together, and  
6           the second plurality of field effect transistors are  
7           p-channel field effect transistors and n-channel field  
8           effect transistors having sources coupled in parallel  
9           together and drains coupled in parallel together.

1           30. The packaged integrated circuit of claim 24 further  
2           comprising:  
3           a switch controller having a mode input, a first  
4           plurality of switch control signals coupled to respective  
5           gates of the first plurality of field effect transistors,  
6           a second plurality of switch control signals coupled to  
7           respective gates of the second plurality of field effect  
8           transistors, the switch controller to control the  
9           switching of the first and second plurality of field  
10          effect transistors.

1           31. The packaged integrated circuit of claim 24 further  
2           comprising:  
3           a plurality of input receivers each having a first  
4           input coupled to the voltage reference node and a second  
5           input coupled to respective data terminals to receive  
6           data.

1        32. The packaged integrated circuit of claim 31, wherein  
2            each input receiver includes  
3            a comparator having a first input coupled to the  
4        voltage reference node and a second input coupled to a  
5        respective data terminal to calibrate a pull-up and a  
6        pull-down of an off-chip output driver.

1        33. The packaged integrated circuit of claim 32, wherein  
2            the comparator of each input receiver further to  
3        receive data by comparing a reference voltage on the  
4        reference node with an input signal on the respective  
5        data terminal.